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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/542,903	07/20/2005	Jason R Hector	GB 030043	1786

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EXAMINER	
HAILEMARIAM, EMMANUEL	
ART UNIT	**PAPER NUMBER**
2629	
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09/10/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/542,903	HECTOR ET AL.	
	Examiner	Art Unit	
	Emmanuel Hailemariam	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/25/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.

(b) CROSS-REFERENCE TO RELATED APPLICATIONS.

(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.

(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.

(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.

(f) BACKGROUND OF THE INVENTION.

(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

(g) BRIEF SUMMARY OF THE INVENTION.

(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING (S).

(i) DETAILED DESCRIPTION OF THE INVENTION.

(j) CLAIM OR CLAIMS (commencing on a separate sheet).

(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).

(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if

the required "Sequence Listing" is not submitted as an electronic document on compact disc).

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. The term "**the pixel data voltage**" in claim 1, lines 11, is a relative term, which renders the claim indefinite. The term "the pixel data voltage " is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

4. The term "**a transistor** " in claim 27, lines 2, is not clear. There are four transistors; it is unclear which transistor the applicant is referring to?

Claim Objections

5. Claim 17 is objected to because of the following informalities:
Claim 17, line 2 recites the " the capacitor arrangement "should have been " the capacitors arrangement ".

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) (Fig. 1,2) in view of Inoue et al. (US 7061452 B2).

AS to claim 1 and 32, AAPA discloses an active matrix device comprising an array of display pixels, each pixel comprising [0002] a current driven light emitting display element [0002]; an amorphous silicon drive transistor [0009] for driving a current through the display element; capacitor (fig. 2)(24) and the drive transistor threshold voltage, (fig. 2, 16 and 22; [008]), but does not disclose first and second capacitors (C1, C2) connected in series that are between the gate and source or drain of the drive transistor a data input to the pixel being provided to the junction between the first and second capacitors thereby to charge the second capacitor to a voltage derived from the pixel data voltage, and a voltage derived from the drive transistor threshold voltage being stored on the first capacitor. However, Inoue, however, discloses first and the second capacitor (fig. 5 (553, 54) connected in series between the source or drain of the drive transistor (see fig. 5) (53 and 52); a data input to the pixel being provided to the junction (fig.5 (51,52; at the junction of 51,52)) thereby to

charge the second capacitor to a voltage derived from the pixel data voltage (col.7 lines 65-67; col.8 lines 1-4), and a voltage derived from the drive transistor (col.2 lines 53-54) threshold voltage being stored on the first capacitor (col.4 lines 4-26).

It would have been obvious for one skilled in the art to combine a first and second capacitors connected in series as taught by Inoue with the device of AAPA because this will provide to store energy, and also uses to charge the second capacitor.

As to claim 2, Inoue discloses a device as claimed in claim 1, wherein each pixel further comprises an input first transistor (fig.5 (53)) connected between an input data line (fig.5 (52) and the junction between the first and second capacitors (fig.5 (553,54)).

As to claim 3, AAPA discloses a device as claimed in claim 1 wherein the drain of the drive transistor (fig.2 (22)) is connected to a power supply line (see fig.2 (26) [0007]).

As to claim 4, Inoue discloses a device as claimed in claim 1, wherein each pixel further comprises a second transistor (fig.5 (55)) connected between the gate and drain of the drive transistor (fig.5 (53).

As to claim 5, Inoue discloses a device as claimed in claim 4, wherein the second transistor (fig.5 (55) is controlled by a first gate control line which is shared between a row of pixels (fig.5 (27)).

AS to claim 6, Inoue discloses a device as claimed in claim 1, wherein the first and second capacitors (fig.5 (553,54)) are connected in series between the gate and source of the drive transistor (fig.5 (53).

AS to claim 7, Inoue discloses a device as claimed in claim 6, wherein each pixel further comprises a third transistor (fig.5 (554)) connected across the terminals of the second capacitor (fig.5) (54)).

AS to claim 8 and 12, Inoue discloses A device as claimed in claim 7, wherein the third transistor is controlled by a third gate (fig.5 (554)) control line which is shared between a row of pixels (fig.2 (27)).

AS to claim 9 and 13, Inoue discloses a device as claimed in claim 8, wherein the second and third gate control lines comprise a single shared control line (col.4 lines 67 col.5.lines 1-16).

AS to claim 10, Inoue discloses a device as claimed in 5 claim 1, wherein the first and second capacitors (fig.5 (553,54)) are connected in series between the gate and drain of the drive transistor (fig.5 (53).

AS to claim 11 Inoue discloses a device as claimed in claim I0, wherein each pixel further comprises a third transistor (fig.5 (554)) connected between the input and the source of the drive transistor (fig.5 (53), col.11 lines 30 -37).

AS to claim 14, Inoue discloses a device as claimed in claim 1, wherein each pixel further comprises a fourth transistor (fig.5 (35) connected between the drive transistor source and a ground potential line (fig.5 (56), col.7 lines 48-50).

AS to claim 15 and 21, Inoue discloses a device as claimed in claim 14, wherein the fourth transistor is controlled by a fourth gate (fig.5 (35) control line which is shared between a row of pixels (fig.2 (27)).

AS to claim 16, Inoue discloses a device as claimed in claim 15, wherein the ground potential line col.7 lines 48-50) is shared between a row of pixels and comprises the fourth gate control line for the fourth transistors (fig.5 (35)) of an adjacent row of pixels (fig.2 (51,57,511).

AS to claim 17, Inoue discloses a device as claimed in claim wherein the capacitor arrangement is connected between the gate and source of the drive transistor (fig.5 (55)), and the source of the drive transistor is connected to a ground line (fig.5 (56).

AS to claim 18, Inoue discloses a device as claimed in claim 17, wherein the drain of the drive transistor (fig.5 (55) is connected to one terminal of the display element (fig.5 (56) the other terminal of the display element being connected to a power supply line (fig.5 (57)).

AS to claim 19, Inoue discloses a device as claimed in claim 17, wherein each pixel further comprises a second shorting transistor connected across the terminals of the second capacitor (fig.5 (553,54)).

AS to claim 20, Inoue discloses a device as claimed in wherein each pixel further comprises a third transistor (fig. 5, (554)) connected between the gate and drain of the drive transistor (fig.5 (53)).

AS to claim 22, Inoue discloses a device as claimed in, wherein each pixel further comprises a fourth charging transistor (fig.5 (35)) connected between a power supply line (fig.5 (57)) and the drain of the drive transistor (fig.5 (53)).

AS to claim 23, Inoue discloses a device as claimed in, wherein each pixel further comprises a second drive transistor (fig.5 (55).

AS to claim 24, inoue discloses a device as claimed in claim 23, wherein the second drive transistor (fig.5 (55)) is provided between a power supply line ((fig.5 (57)) and the first drive transistor (fig.5 (53)).

AS to claim 25, Inoue discloses devices claimed in claim 24, wherein the gate and drain of the second drive transistor (fig.5 (55)) are connected together (fig.5 (53)).

AS to claim 26, Inoue discloses a device as claimed in claim 23, wherein the second drive transistor (fig.5 (55)) is provided between the first drive transistor (fig.5 (53)) and the display element ((fig.5 (56), (col.8 lines 58-60)).

AS to claim 27, Inoue discloses a device as claimed in claim 26, wherein a transistor is connected between the gate and drain of the second drive transistor (fig.5) (55)).

AS to claim 28, Inoue discloses a device as claimed in claim 26, wherein each pixel further comprises a fourth transistor (fig.5 (35)) connected between the gate of the second drive transistor (fig.5 (55), and a ground potential line. (fig.5 (56), col.7 lines 48-50).

AS to claim 29, Inoue discloses a device as claimed in claim I, wherein the drive transistor comprises an n-type transistor. (Fig.5)(55)).

AS to claim 30, Inoue discloses a device as claimed in claim I, wherein the display element comprises an electroluminescent display element (col.1 lines 19-26).

AS to claim 31, Inoue discloses a device as claimed in claim 30, wherein the electroluminescent display element comprises an electro phosphorescent organic electroluminescent display element (col.1 lines 19-26, col.12 lines 41-45).

AS to claim 33, Inoue discloses a method as claimed in claim 32, wherein the step of charging a second capacitor (fig.5 (54) is carried out by switching on an address transistor connected between a data line (52) and an input to the pixel (see.fig.5).

AS to claim 34, Inoue discloses a method as claimed in claim 33, wherein the address transistor for each pixel in a row is switched on simultaneously by a common row address control line (see.fig.17).

AS to claim 35, Inoue discloses a method as claimed in claim 34, wherein the address transistors for one row of pixels are turned on substantially immediately after

the address transistors for an adjacent row are turned off (see fig.5; fig.5 (57), (fig.5 (51).

As to claim 36, Inoue discloses a method as claimed in claim 32, wherein the first capacitor (fig.5 (553) of each pixel is charged to store a respective threshold voltage of the pixel drive transistor at an initial threshold measurement period of a display frame period a pixel driving period of the frame period following the threshold measurement period (col.4 lines 10-26) the optimum boundary of the voltage).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Hailemariam whose telephone number is 571-270-1545. The examiner can normally be reached on M-F 8:00am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare

Mengistu can be reached on 571-270-1550. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Emmanuel Hailemariam 08/16/07

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER